S-Interface Protection Recommendations

for the

Am79C30A Digital Subscriber Controller

Advanced Micro Devices
ISDN Systems Engineering

Protecting the S-Interface from exposure to electrical surge is an important system consideration for design and implementation of ISDN Terminal Equipment. A recommended solution is presented, as well as a background of the performance restrictions.

Introduction

Design of protection circuitry for ISDN S-Interface equipment can become a challenging problem if the equipment needs to meet the performance requirements as well as maintain reliability from exposure to electrical surge. ISDN TE's typically are installed and wired within buildings and usually do not have their conductors routed outside as is typical with analog lines. This installation limits the electrical exposure to a point, but possibilities exist for interface bus conductors to be exposed to electrical surge or power fault energies. Examples of these voltages are from accidental S-bus connection to power mains, inadvertent connection to analog voice telephone lines where battery feed or ringing voltages may be present, or from induced electrical (lightning) surge. With exposure of the S-Interface bus to these voltage levels, the designer must ensure protection of the user and surroundings, protect the TE itself from damage or reliability impairment, and prevent degrading network performance.

Not only must the system be unaffected by repeated transients upward to 1000 volts, but the circuitry that provides this protection must not itself degrade normal system performance. The ISDN S-Interface Layer 1 operational requirements are identified in the CCITT I.430 and ANSI T1.605 specifications. Performance requirements of these specifications impose several restrictions on the methods that can be used for surge protecting ISDN S-Interface Terminal Equipment. While CCITT I.430 does not address needs for protection from electrical exposure, its operational requirements pose restrictions on acceptable methods of protection. ANSI T1.605 identifies nearly the same operational requirements, but additionally addresses electrical exposure.

Internal circuit connections are normally designed to be inaccessible to the user by an overall enclosure. Electrical shock to the user from externally-applied S-Interface faults is best prevented by choosing components with sufficiently high dielectric ratings. In ISDN TE designs, the termination resistor on the bus is not usually part of the TE. If the application, however, requires the 100 ohm bus termination within the unit, power dissipation under fault conditions must then be considered. Even if measures are taken to eliminate safety hazards to the user, the equipment must continue to operate after surge exposure. The addition of protection circuitry is recommended to prohibit possibilities of these external energies from damaging the Am79C30A.

Protecting the Am79C30A's LIU

Internal protection is typically designed into integrated circuit devices to help limit permanent internal destruc-

tion resulting from externally applied voltages outside of the normal operating range. These methods usually consist of internal diodes from the pin connection to supply or ground. Although reversed biased during normal operation, the diodes begin to conduct and clamp voltages that fall below ground or rise above the power supply level. However, when the applied energy can be greater than this internal protection can accommodate, an external protection network can restrict the magnitude of this energy such that it can be safely handled by the device.

Protection Effects on Performance

The CCITT and ANSI standards specify pulse shape and impedance templates that restrict the loading that can be placed across the line. This loading limit restricts total capacitance, neglecting any other impedances, to less than 800 picofarads. A connecting cord is allowed to contribute up to 350 picofarads of the total impedance. Varistors typically have capacitance in the range of nanofarads which precludes their use across the line. Transformers have internal reactive impedances, primary inductances, and distributed and interwinding capacitances. An equivalent reactive network is formed by the transformer inductance and capacitance, the connecting cord capacitance, plus any other capacitive elements caused by the protection devices. Depending on values of these elements, there is potential for distorting pulse shapes beyond the allowable template limits.

The 96KHz test requires the resulting current from an externally applied 1.2 volt peak voltage to be below 0.6 milliamp. This comparatively high voltage is more likely to cause clamping diodes to conduct than the lower 100 millivolts used during impedance tests, especially if diodes are placed across the DSC side of the transformer where this applied voltage appears as 2.4 (1.2 volts x 2) peak volts. The impedance tests are also required to be met when the TE is powered down, to ensure that an unpowered TE in a multipoint environment does not load the line. Any protection scheme that is referenced to Vcc must allow for Vcc to become a DC ground when power is removed.

Elements of Protection Networks

Transformer characteristics have a high control over pulse shapes and impedance. High leakage inductance can lead to overshoot or ringing problems on the pulse shape edges. Winding capacitances add to the total load capacitance across the line, and must also be carefully controlled. Impedances reflect across the transformer by the turns ratio squared, so any impedance on the line side is multiplied by four when seen at the DSC side of the transformer. The Appendix at the end of this document contains additional transformer information and specifications.

Capacitance as seen at the line is the total of all line side capacitances from the connecting cord and transformer winding capacitance, plus four times (one fourth of the impedance) the total capacitance that appears across the DSC side of the transformer.

Series resistors from the DSC output pins are used to match the impedance and voltage the transmitter output to that of the line through the transformer. Resistors are also used at the input pins, but primarily for current limiting during the 96 KHz tests. These resistors on both input and output also serve to current limit the surge energies coupled across the transformers from the line. Therefore their power dissipation capability must be considered.

Diodes to clamp voltage transients must not conduct during normal operation, nor during the 96 KHz tests. They must not present a high capacitance in their non-conducting state. Schottky diodes, often desired for their quick turn-

on and low forward voltage, exhibit too high a capacitance to be considered. Zener type devices also have high capacitance and possibly high leakage, although these drawbacks can be controlled by series connection with another diode having low junction capacitance. Since surge energy is routed through diodes, their transient power capabilities must be sufficiently high and their conducting resistance must be low. However, capacitance of a diode typically increases as its power capability increases, limiting the choice of diodes that can be used.

The DSC outputs Lout1 and Lout2 operate as a pair to differentially drive pulses of opposite polarities into the transformer. During the generation of a "mark" (zero) the DSC provides a low impedance differential output voltage of ±2.326 volts to the transformer. A "space" (one) on the bus is defined as a high differential impedance from the drivers such that the differential line voltage goes to zero due to the line termination resistors. This high impedance state required during a "space" condition can cause ringing and overshoot and requires limiting the reactive elements of the line interface.

Since a TE on a bus cannot present any signal loading when it is powered down, the outputs must remain at a high impedance state. Because of this requirement internal device protection diodes connected to internal Vcc cannot be used. In the powered off state, Vcc becomes a DC ground and internal diodes to Vcc would conduct and would present signal loading to the bus. Internal protection diodes to ground, however, are included. A simplified representation of the DSC's output is shown in Figure 1.

The outputs operate within a voltage range of 0 to +2.326 volts. At approximately + 12 volts, reverse breakdown of the internal diodes occurs, and at approximately -0.5 volts forward conduction occurs. Reverse voltage breakdown should be avoided if at all possible, but forward

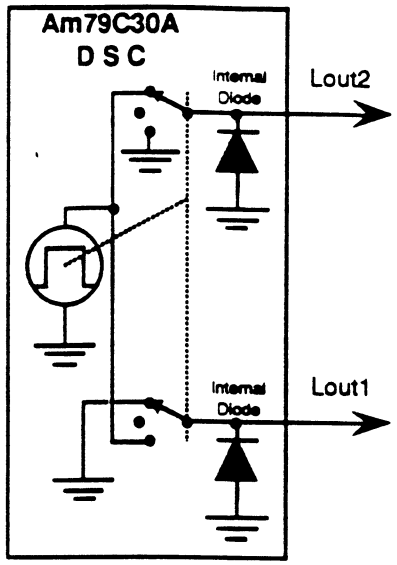

Figure 1.
Simplified DSC Output Representation

conduction is allowed if the current into the pin is maintained below 10 milliamps to avoid device latchup.

The DSC inputs Lin1 and Lin2 operate as a true differential high impedance (approximately 20 Kohm) input. Current limiting resistors are connected between the transformer and these inputs which solves the loading problems of the bus when power is removed from the TE. This allows the use of internal protection diodes to internal ground and to internal Vcc. These diode structures to Vcc and Vss are internal to the chip and begin to forward conduct at approximately 0.5 volts. The surge currents on Lin1 and Lin2 are limited by external resistors.

Internal DC biasing places the nominal operating voltage of these inputs at 1/2 of Vcc, where they appear as inputs to an op-amp. Under normal operating conditions, the greatest input voltage will occur at short loop length. This will produce voltages of approximately +2.5 ± 1.5 volts, where the nominal operating point of 2.5 volts represents a "space" and ei-

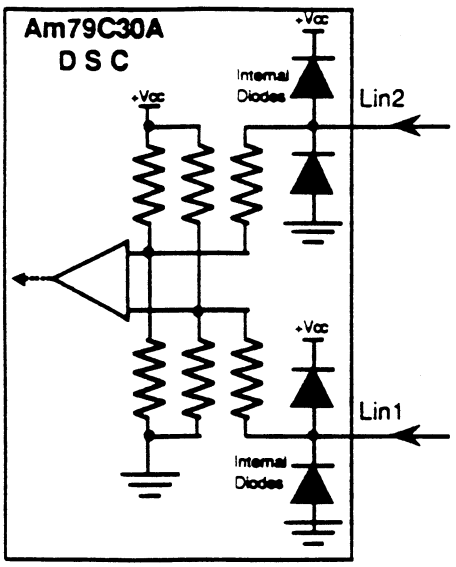

Figure 2.
Simplified DSC Input Representation

ther 1.0 volt or 4.0 volt represents a "mark". A simplified representation of the DSC's input is shown in Figure 2.

Layout and Component Placement for Optimum Protection

Physical placement of the protection network plays an important part in its effectiveness. During a surge, the external voltages can be quite high, leading to potentially high currents through these diode voltage-clamp networks. Not only must the diodes be sized to handle this current, but careful layout and sufficient circuit sizing must be exercised to lower the total voltage drop across the conductor path during presence of high current.

Recommended Protection Solution

A recommended protection circuit implementation for the Am79C30A DSC is shown in Figure 3 and the related components are listed in Table 1. Recommended transformer part numbers are listed in Table 2 in the Appendix. Although relatively simple, several points should be noted about this circuit. Separate protection is used for the receive (Lin) and the transmit (Lout) circuits. In both cases, notice that surge energy is dumped only to ground and not to Vcc. This is done for two reasons: First, if the device is in the powered down state, Vcc is at ground potential. A single diode voltage drop to this grounded Vcc causes excessive signal loading on the S-bus, and therefore causes failure of the impedance tests. Second, it is generally recommended to avoid dumping surge energy to any supply voltage path, since other devices share the same power and have the potential to be damaged with undue transients on their power bus.

A zener diode in series with another diode is used to shunt positive transients to ground. The series diode (D2 or D4 for Z1, and D6 or D8 for Z2) is chosen for its low capacitance, which isolates the zener's high capacitive loading. The conduction breakdown point is sized in order to accommodate the operating signal ranges that normally appear on the lines being protected. Due to possibilities of performance degradation during normal operation, a separate zener for each input and output is used. A single zener common to both the transmit and receive protection networks is not recommended.

In this protection scheme, the series resistance from Lin or Lout to their transformers is split into two resistors and the protection diodes are placed at this splitting point. By placing one of the resistors (R2a, R2b, R4a, or R4b) between the transformer and clamping diodes, that resistor aids in reducing total current and dissipation requirements of the diodes during a surge.

The clamped voltage at the protection diodes can easily be greater than the clamping values of the Am79C30A's internal pin clamping diodes, leading to current flow into the pins. This current can be calculated from dividing the difference between the external clamp volt-

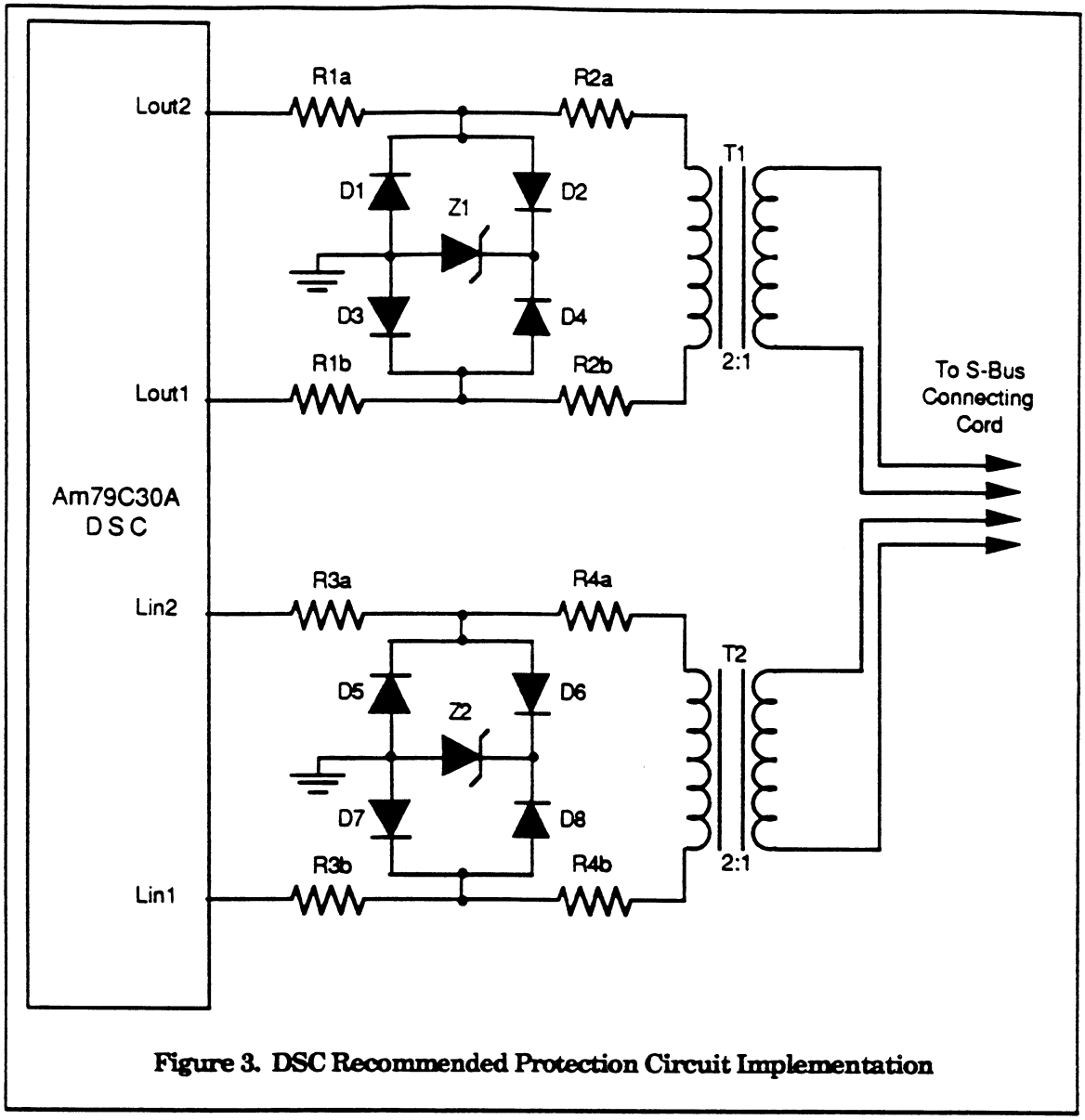

Figure 3. DSC Recommended Protection Circuit Implementation

Device	Number	Type
D1, D2, D3, D4	MUR120	Diode
D5, D6, D7, D8	1N4448	Diode
Z1	1N5337A	4.7V, 5 watt zener diode
Z2	1N4733 A - 3	5.1V, 1 watt zener diode
Z3	1.5KE56	Transzorb™
D9, D10, D11, D12	1N4004	Diode
R1a, R1b, R2a, R2b	22.6 ohm, 0.5 watt, 1%	Resistor
R3a, R3b	2.0 Kohm, 5%, 0.25 watt	Resistor
R4a, R4b	3.6 Kohm, 5%, 0.25 watt	Resistor
T1, T1	(See Table 2)	Transformers

Table 1. Components for Recommended Solution of Figure 3

age and the internal clamp voltage by the connecting resistance. This resistance, which limits current into the DSC, is the second of the split resistor pair, R1a,b at the outputs and R3a,b at the inputs.

Protection Diode Selection

Output Protection Diodes: Surge transients can occur either as longitudinal (common mode) or metallic (differential) voltages, coupled across the transformer by magnetic coupling, interwinding capacitance, or both. The objective of the protection network is to limit the voltage at each pin. Longitudinal surges will enter both leads together and are bypassed to ground. Metallic surges will travel through the diode network but the maximum voltage at any point is limited by the network shunting to ground.

Operation of this protection circuit occurs differently depending on the surge polarity. A negative surge travelling from the transformer T1 to Lout2 in Figure 3 will forward bias diode D1. A positive surge, however, travels through diode D2, where it is clamped to ground by the zener voltage of diode Z1. Z1 is a 1N5337A 4.7 volt zener diode. Considering tolerance variations and forward drop from surge currents, this zener and series diode arrangement provides a positive 6 to 7 volt clamping limit. This is still well below the reverse conduction point of the DSC's outputs. A zener diode with a voltage rating lower than this can begin to exhibit high leakage, possibly causing the series diode to begin to conduct and thereby affect the pulse shapes. A higher voltage rating raises the positive clamping point, which must be considered for DSC reverse conduction when the TE is in the powered down state. This particular 5-watt zener diode was also chosen due to its low conducting resistance which reduces the clamped voltage level.

Diodes D1 through D4 are MUR120. This fast switching diode can handle relatively high short duration surges, but most importantly, offers a junction capacitance much lower (typically 20 picofarads) than other diodes of comparable power ratings. The total capacitance with this arrangement has shown a negligible effect on impedance or pulse shape measurements, using the components referenced in Figure 3 and Table 1.

Input Protection Diodes: The input protection network operates identically to that of the output, except for component values and device choices. Since the inputs are high impedance, series resistance can be added without degrading operation.

The DSC inputs have internal pin protection diodes connected to internal Vcc as well as to internal ground. One of these will begin to forward conduct if the pins are exposed to voltages approximately 0.5 volt below ground or 0.5 volt above Vcc. (Remember that if power is removed, Vcc is zero volts.) If the external protection diodes clamp voltages from an external surge to a finite voltage limit, the series resistors between the protection diodes and the DSC will limit this current to a safe value.

Diodes D5, D6, D7, and D8 are 1N4448 switching diodes. These diodes have very low off-state capacitance, and since higher value resistors (R4a, R4b) are used from the transformer, surge current is limited to a value within these diodes' capability. Since the DSC inputs operate at a nominal +2.5 volts with applied signal pulses as high as ±1.5 volts, the zener diode Z2 must not begin conducting until above this limit. From worst case assumptions, if Vcc varies by 5% the DSC's internal midpoint (comparator reference) voltage can increase to approximately 2.75 volts. If the ±1.5 volt signal can vary up to 10%, the highest voltage seen by either lead to the inputs could be as high as 4.4 volts. Assuming a zener can vary by up to 10%, the combined zener plus forward diode drop must be above this 4.4 volt limit. The

zener and diode will typically begin high impedance conduction slightly below the zener knee, and if too low, can begin to attenuate the received signal peaks. A 5.1 volt zener (1N4733) was chosen to ensure this conduction point is high enough to prevent attenuation while keeping the clamping point at its lowest possible value.

Series Resistor Selection

Output Series Resistors are calculated to obtain the required 0.75 volt signal pulses when the S-Interface is terminated into a 50 ohm test load, where 50 ohms represents the combined effect of the two 100 ohm terminating impedances on the bus. The Am79C30A's nominal output voltage of 2.326 volts is reduced by the transformer winding ratio and series resistance in the path. Figure 4a shows a representation of the significant elements in obtaining the desired load voltage. Elements which must be considered are the winding resistances of the transformer, the DC resistance of the connecting cord, and the specified bus termination. If any other element is required in the path before connection to the termination resistor, it too must be included in the calculation. The relatively low output impedance of the DSC during an active mark state is not considered for these calculations, as the DSC's output voltage is specified into a load representative of normal loaded conditions. Figure 4b shows the significant elements for calculating the series resistance, simplified by omitting the transformer and reflecting all line-side values to the DSC side of the transformer. The total series resistance is calculated in the example in Figure 4.

For a transformer with 2.2 ohm primary and 5.0 ohm secondary DC resistances, and a connecting cord of 1.2 ohms (7 meters of #24 AWG), the total R_{series} is equal to 91.5 ohms. Since the inputs and outputs of the DSC operate differentially, the chosen resistor values are divided in half across the differential DSC connections to help maintain a symmetrical signal balance. For the output leads, the protection diode network is placed midpoint from transformer to DSC. The net individual resistor values are therefore equal to $(1/4)R_{series}$, or in this case = 22.88 ohms. The closest 1% resistor value is 22.6 ohms which is the choice for R1a, R1b, R2a, and R2b.

Input Series Resistors: The primary concern for resistors on the input circuit is to not load the S-Interface bus during the 96KHz test or when the TE is in the powered down state. When the DSC is powered down, a path to ground is provided by the internal protection diodes for signals of either polarity. If the 1.2 volt peak 96 KHz signal is applied to the line connection, this voltage would appear as 2.4 volts across the Lin pins. However, this does not occur since 2.4 volts is above the forward conduction point for these internal diodes. In order to limit this current to the maximum specified (0.6 milliamps at the line side) sufficient series impedance must appear in the path. This series resistance must, however, limit the current to less than the maximum allowed since other components in the system also draw current contributing to the 0.6 milliamp limit during this 96 KHz test. The significant elements include the connecting cord capacitance, transformer distributed capacitance, and transformer primary inductance. A model of this equivalent circuit is shown in Figure 5a, where the DSC is assumed to be in a powered down state. The internal diodes have a nominal forward conducting voltage of approximately 0.5 volt. For either polarity of the input signal, two of these diodes will always be forward biased when the presented voltage is sufficiently increased. At the DSC side, this voltage is approximately 1.0 volt with the two diodes acting in series. Reflected to the primary side of the transformer this becomes 0.5 volt. The total series resistance also reflects to the primary side as one fourth of its value.

Assuming the connecting cord is at its maximum specification capacitance of 350 picofarads and the trans-

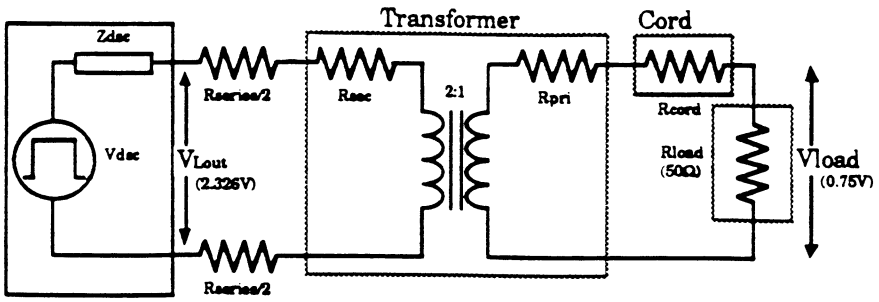

Figure 4a. DSC Output Series Resistance Model

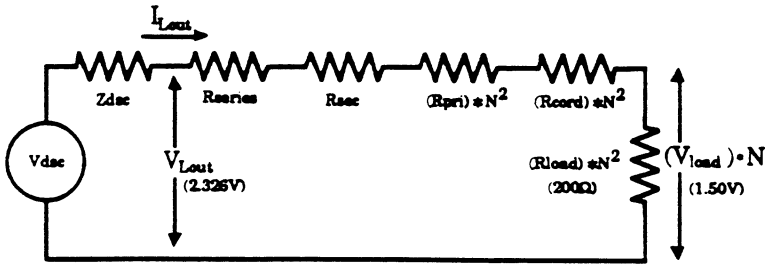

Figure 4b. DSC Output Series Resistance - Simplified Equivalent Circuit With All Elements Reflected to the DSC Side of the Transformer

To obtain the specification-required 0.75 volt pulse across the line into 50 ohms, the current at the DSC's output must be $\frac{1}{2}\left(\frac{0.75 \text{ volt}}{50 \text{ ohm}}\right)$ = 7.5 milliamps.

From Figure 4b, the current, I_{Lout}, is:

$$I_{Lout} = \frac{V_{Lout}}{R_{series} + R_{sec} + R_{pri} \bullet N^2 + R_{cord} \bullet N^2 + R_{load} \bullet N^2}$$

where:

N is the transformer turns ratio, 2:1, DSC-to-line side,
R_{sec} is the DC resistance of the DSC side of the transformer,
R_{pri} is the DC resistance of the line side of the transformer,
R_{cord} is the DC resistance of the TE connecting cord,
R_{load} is the S-Interface termination impedance of 50 ohms,
V_{Lout} is the nominal DSC line driver output voltage, 2.326 volts, at rated loading.

The total resistance, R_{series} is then calculated as:

$$R_{series} = \left[\frac{V_{Lout}}{I_{Lout}} - R_{sec} - \left(R_{pri} \bullet N^2\right) - \left(R_{cord} \bullet N^2\right) - \left(R_{load} \bullet N^2\right)\right]$$

Figure 4. Output Series Resistor Calculations

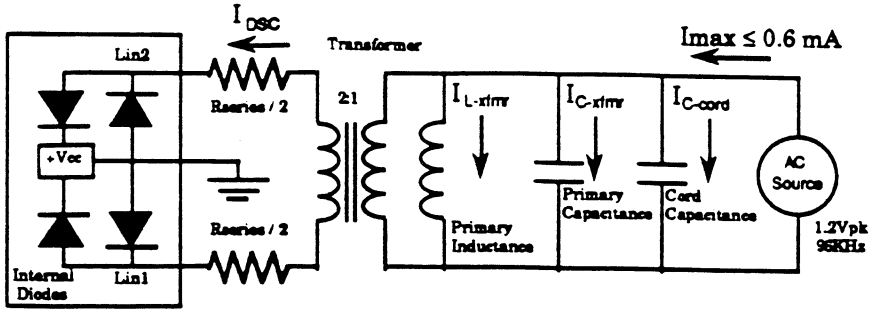

Figure 5a. DSC Input Series Resistor Model

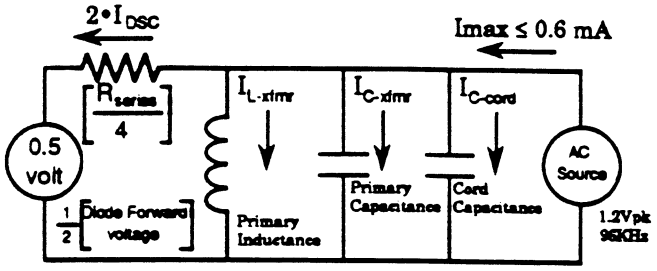

Figure 5b. DSC Input Series Resistance - Simplified Equivalent Circuit With All Elements Reflected to the Line Side of the Transformer

Resistor calculations, reflecting all elements to the line side of the transformer:

With the 1.2 volt 96 KHz signal presented across the line:

I_{cord} becomes 0.26 milliamp

$I_{C\text{-}xfmr}$ becomes 0.13 milliamp, and

$I_{L\text{-}xfmr}$ becomes 0.07 milliamp.

$I_{C\text{-}xfmr}$ and $I_{L\text{-}xfmr}$ partially cancel due to opposite current phases, and allowing for a worst case phase relationship of the cord current compared to the DSC current, an allowable current for the DSC is reduced to:

[0.6 ma - 0.26 ma - (0.13 ma - 0.07 ma)] = 0.28 milliamp, represented by $2 \bullet I_{DSC}$

From this maximum current, R_{series} becomes 10.0 Kohms.

Allowing for variations of these elements plus resistor tolerance, R_{series} is chosen as **11.2 Kohms**.

Again dividing this equally for L_{in1} and L_{in2},

$\frac{R_{series}}{2}$, the resistors for each lead at L_{in1} and L_{in2} each become **5.6 Kohms**.

This 5.6 Kohms is obtained with two resistors of 3.6 Kohm and 2.0 Kohm in series. The protection diode network is then placed at this splitting point.

Figure 5. DSC Input Series Resistor Calculation

former has 180 picofarads of capacitance and 28 millihenries of inductance, the minimum resistance calculations are shown in Figure 5.

To limit current into the protection network during surge conditions, the series resistance is divided between the transformer and the DSC. The total of 5.6 Kohm is realized with standard 5% resistors of 2.0 Kohm and 3.6 Kohm. The larger 3.6 Kohm resistors are placed on the transformer side (R4a and R4b in Figure 3) allowing for greater surge current limiting.

Summary

Proper consideration of line interface protection during the initial design can minimize cost and effort of resolving both protection and system operational problems later in the development cycle. Choices of protection may be dictated by the system's intended application but loading effects of protecting devices and their possible degradation to line performance must always be considered. Equivalent models of the network can be constructed for a mathematical analysis and their results are usually predictable. However, actual testing with careful measurement of transient levels is necessary to ensure that device limits are not exceeded and reliability is not compromised. Key issues consider are:

- Understand the magnitudes of external surge energy and their methods of connection to the S-reference point.
- Determine the maximum allowable capacitive loading that may be placed across the DSC's LIU input and output lines without exceeding performance limits.
- Calculate series resistance values and determine their surge current limiting effects for the energies expected in the design's environment.
- Choose devices (diodes) to bypass the surge current to ground based on their capacitance, forward resistance, and dissipation characteristics.
- Perform surge testing on the design and measure any voltages or currents that can possibly enter the devices being protected. Be sure that the energy across the device is actually limited, not simply the voltage across the protection network.

References

- "Am79C30A Device Data Sheet", AMD Publication #09893E.
- "Key Design Hints for the (Am79C30A) DSC", AMD Publication # 12618.
- "Electromagnetic Compatibility Design Considerations for ISDN Terminal Equipment", AMD Application Note.
- "ISDN User-Network Interfaces: — Layer 1 Recommendations", CCITT Recommendation I.430.
- "Integrated Services Digital Network (ISDN) — Basic Access Interface for S and T Reference Points (Layer 1 Specification)", ANSI Standard T1.605-1988.
- "Lightning and 60 Hz Disturbances at the Bell Operating Company Network Interface", Bell Communications Research, Technical Reference TR-EOP-000001, Issue 1, June, 1984.

Appendix

Specifications and Regulatory Standards for ISDN Terminal Equipment

CCITT recommendation I.430 defines operational performance parameters for ISDN S-Interface equipment. ANSI T1.605, developed from I.430, includes the original CCITT requirements, but also adds requirements for the US telecom market, including performance from exposure to voltage faults. The ANSI T1.605 standard specifies two categories of protection requirements. One is for external voltage isolation protection to ensure no fire or shock hazard is created by a TE. The other protection category, where continued operational reliability is required, addresses accidental misconnection of TE's to other non-ISDN voltages, or exposure to induced electrical surge.

On safety issues, the T1.605 document refers to the UL Standards 1459 and 478. Accidental connection of an ISDN TE to an analog phone line exposes the interface to the DC voltage feed or to AC ringing voltage. The ANSI document requires ISDN TE's to withstand 5 minute exposure to a 56.5 volt DC source, limited to 0.5 amp, or a 20 Hz 200 volts peak AC source, alternating 2 seconds ON and 4 seconds OFF (ringing cadence), with 1500 ohms series resistance. Induced surge susceptibility is specified for repeated applications of ±1000 volt, 1x50 waveform surges. (The "1x50" designation describes the waveshape to have a 1 microsecond rising edge and a decay to 50% of its magnitude in 50 microseconds.)

Depending on the location where ISDN Terminal Equipment is to be used, there may be additional regulatory standards that specify minimum performance or safety issues. These standards may be government dependent or may be operational guidelines for the expected user environment. The Am79C30A is designed to be compliant to the recommendations of ISDN standards. The system designer must be aware of any other environment the designed equipment will be operated within and what regulatory standards apply. The designer is responsible to ensure conformance to those standards.

Transformers

Transformer parameters can have a significant effect on protection performance. A sufficiently high dielectric rating will prohibit insulation breakdown and direct connection of externally applied voltages to internal circuit paths. Even without this breakdown, surge transients are coupled across the transformers by magnetic coupling, interwinding capacitance, or both. These impedances, plus those of winding resistances aid to limit the surge current that must be shunted to ground by protection schemes. System performance requirements, to meet pulse template and impedance specifications, dictate minimum transformer parameters. The leakage inductance of the transformer must be kept very low (nominally 10 to 12 microhenries) in order to avoid overshoot or ringing problems on the pulse shape edges. These performance parameters are usually the first to be considered in making a transformer choice but then must also be considered for surge protection.

Samples from the manufacturers shown in Table 2 have been tested for conformance to CCITT I.430 and ANSI T1.605. Although samples are confirmed to meet or exceed the requirements of CCITT/ANSI, no guarantees are implied. Transformers from other manufacturers are available but have not been verified with the Am79C30A DSC. The performance-related transformer parameters that can also be considered for protection network design are listed in Table 3.

Manufacturer	Part Number	Package
Pulse Engineering	PE-64999	Single
Pulse Engineering	PE-65499	Dual
BH Electronics, Inc.	500-~~1645~~ 1720	Single
BH Electronics, Inc.	500-1717	Dual
Vacuumschmelze	402/521-52-261	Single

(Dual package devices contain two identical transformers each for transmit and receive.)

Table 2. Transformers for Recommended Solution

Parameter	Measurement	Min	Max	Units
Primary Inductance	Measured across primary with secondary open	22		mH
Leakage Inductance	Measured across secondary with primary shorted		11	µH
Distributed Capacitance	Measured across primary with secondary open		180	pF
Interwinding Capacitance	Measured from shorted primary to shorted secondary		130	pF
Primary Resistance	DC measurement across primary (S-bus side)		3	Ohms
Secondary Resistance	DC measurement across secondary (DSC side)		5	Ohms

Table 3. Minimum Transformer Parameter Specifications

Phantom Power Feed Considerations

A phantom power feed scheme (CCITT/ANSI designated Power Source 1) is shown in Figure 6, where operating power is fed through the S-bus transmit and receive pairs. This power is connected from the transformers' center taps to a DC-DC converter, which supplies the necessary operating voltage for the circuit. In this scheme, the power is connected in a similar center-tapped arrangement on the network side (NT) of the S-interface.

If a phantom power feed arrangement is to be used, the DC-DC converter can also be exposed to externally applied surge energy. From Figure 6, the diode bridge using 1N4004 general purpose rectifier diodes, provides the polarity steering to both the DC-DC converter and the unipolar Transzorb™. Protection of the DC-DC converter is accomplished by the clamping action of the Transzorb™ avalanche protector diode. A 56 volt Transzorb™ was chosen since this voltage is well above the externally applied maximum design voltage for phantom power feeding and is below the maximum ratings of the DC-DC converter. Internal dielectric protection within the DC-DC converter should be high enough to block surge transients from traveling from its input to output terminals.

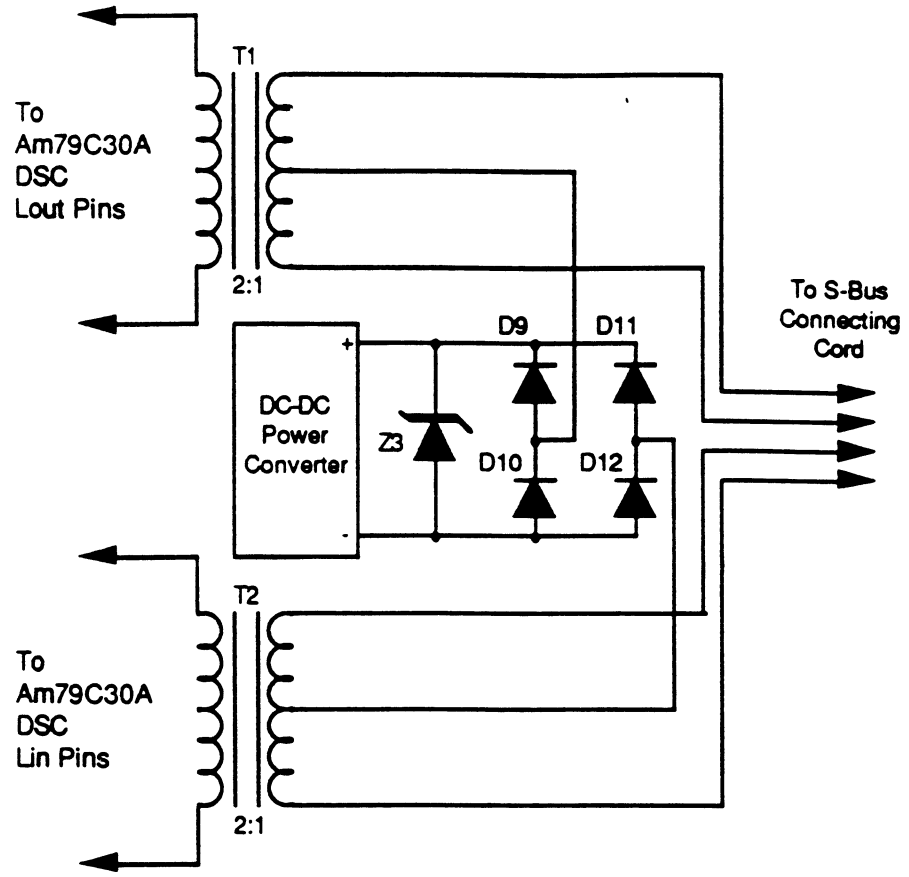

Figure 6. Phantom Power Feed Arrangement

EMI – Electromagnetic Interference

ISDN equipment often utilizes high speed digital processing within the same areas which interface to external busses. While the Am79C30A's S-Interface signal itself presents virtually no contribution to radiated emissions, other digital circuitry within a CPE may be of concern. Due to fast switching edges, digital signals typically encountered in processor-based systems can easily generate frequencies that are orders of magnitude above data rates. Depending on system architecture and design, common mode coupling to an external connecting cord may cause the cord to act as an antenna. This allows internal high frequencies to emanate from the system and produce emission levels above the limits set by regulatory agencies. In this situation, a means to limit EMI may be desired in the interfaceing circuitry to the S-reference connection point.

If it is determined that measures to reduce EMI are required for the particular design, one effective means to limit such emissions is to use inductive chokes in series with the outgoing leads. This inductance appears as a high impedance to frequencies of concern and prohibits them from traveling through the cord. However, this added inductance can also lower the system performance similar to the effects of high capacitance from pro-

tection networks. Surge protection schemes for the S-Interface are chosen to have minimal effect on normal system performance. If it is necessary to include a filtering scheme to limit radiated emissions, that scheme must also not affect system performance. The scheme shown in Figure 7 is recommended. It uses a multiple winding common mode choke. Since the radiated emission signals occur equally as common mode signals to all conductors, a single 4-winding choke can be used for all four interface conductors of the transmit and receive pairs. If the windings are closely matched, differential mode inductance becomes very small and crosstalk between transmit and receive pairs is negligible.

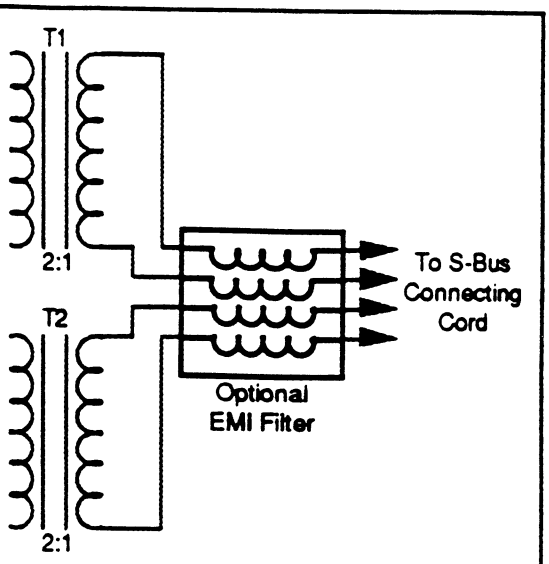

Figure 7.
Common Mode Choke EMI Filter